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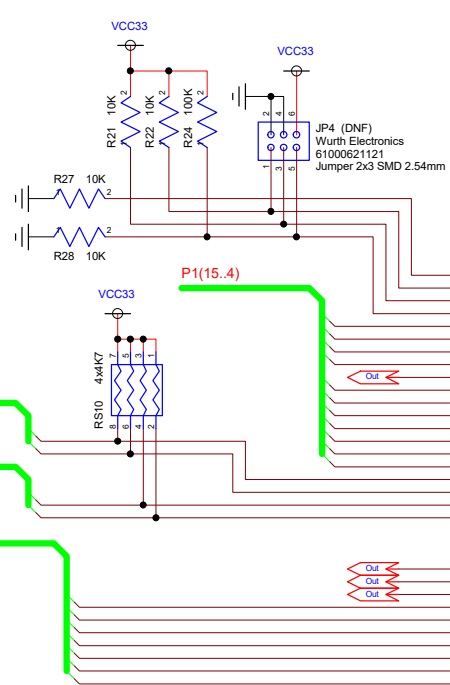
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PAGE	DESCRIPTION
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03	MCU - POWER
04	MCU - OTHER CONNECTIONS (USB, CRYSTAL, JTAG...)
05	POWER
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07	UART - USB
08	MEMORY - SD
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 Owned by www.renesas.eu	PRODUCT	STREAM-IT - RZ/A1L BOARD LAYOUT			DRAWN BY	PATRICK S.	DATE	2016.08.10
	PAGE	INDEX			APPROVED BY	TOLENTINO M.	DATE	
 Designed by www.m13design.fr	REFERENCE	VERSION	REV	REMARKS		DATE	SIZE	SHEET
	REN0001 1402	V2.3		DNF : Dot Not Fit		2017.09.25	A4	01 OF 13



CLOCK TABLE		
MD_CLKS	MD_CLK	MODE
0		SSCG DISABLED (DEFAULT)
1		SSCG ENABLED
	0	EXTAL
	1	USB_X1 (DEFAULT)

BOOT TABLE		
MD_BOOT1	MD_BOOT0	BOOT MODE
0	0	CS0=16bit
0	1	SD
1	0	SPI (DEFAULT)
1	1	MMC

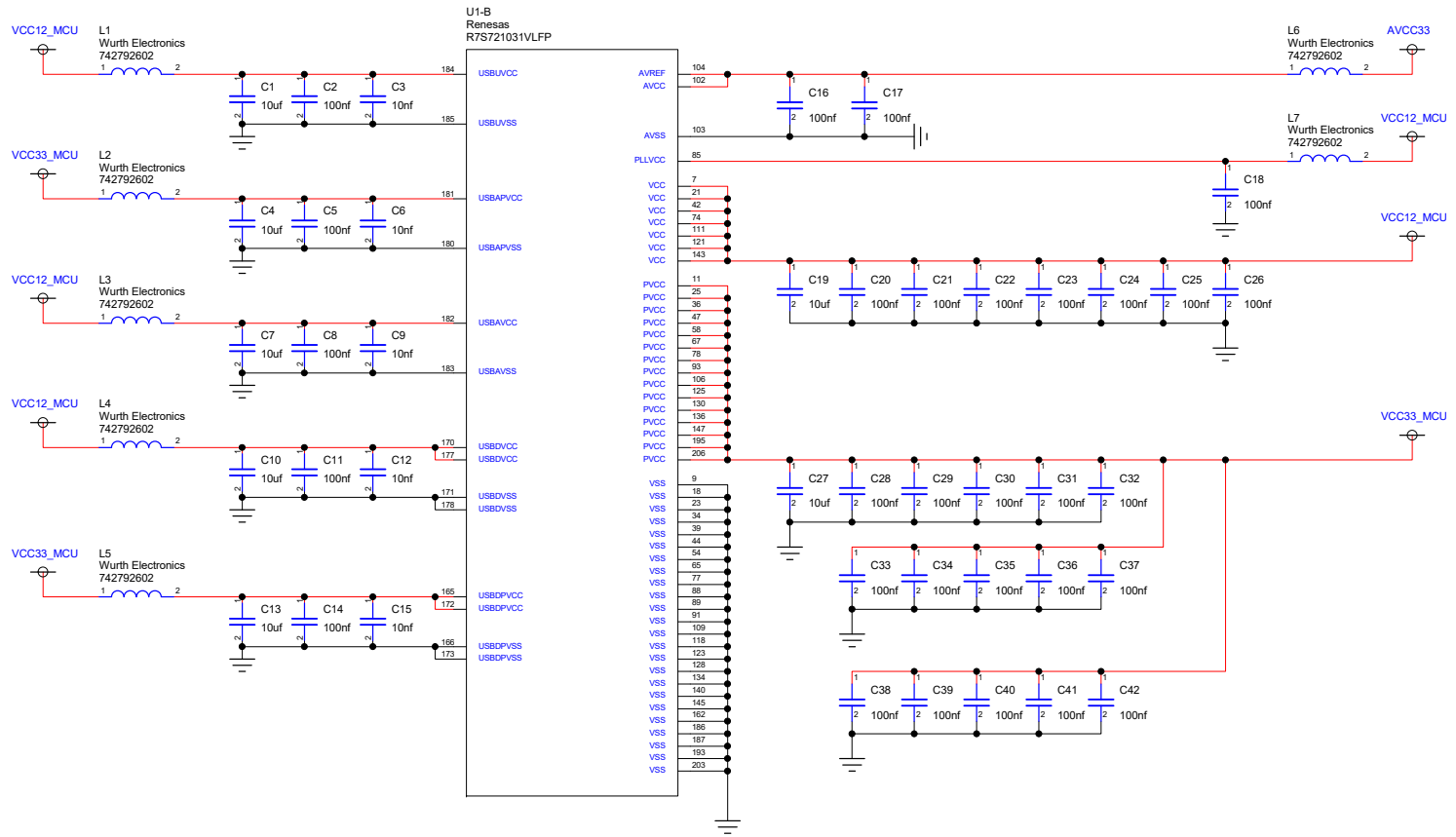
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R7S721031VLPF

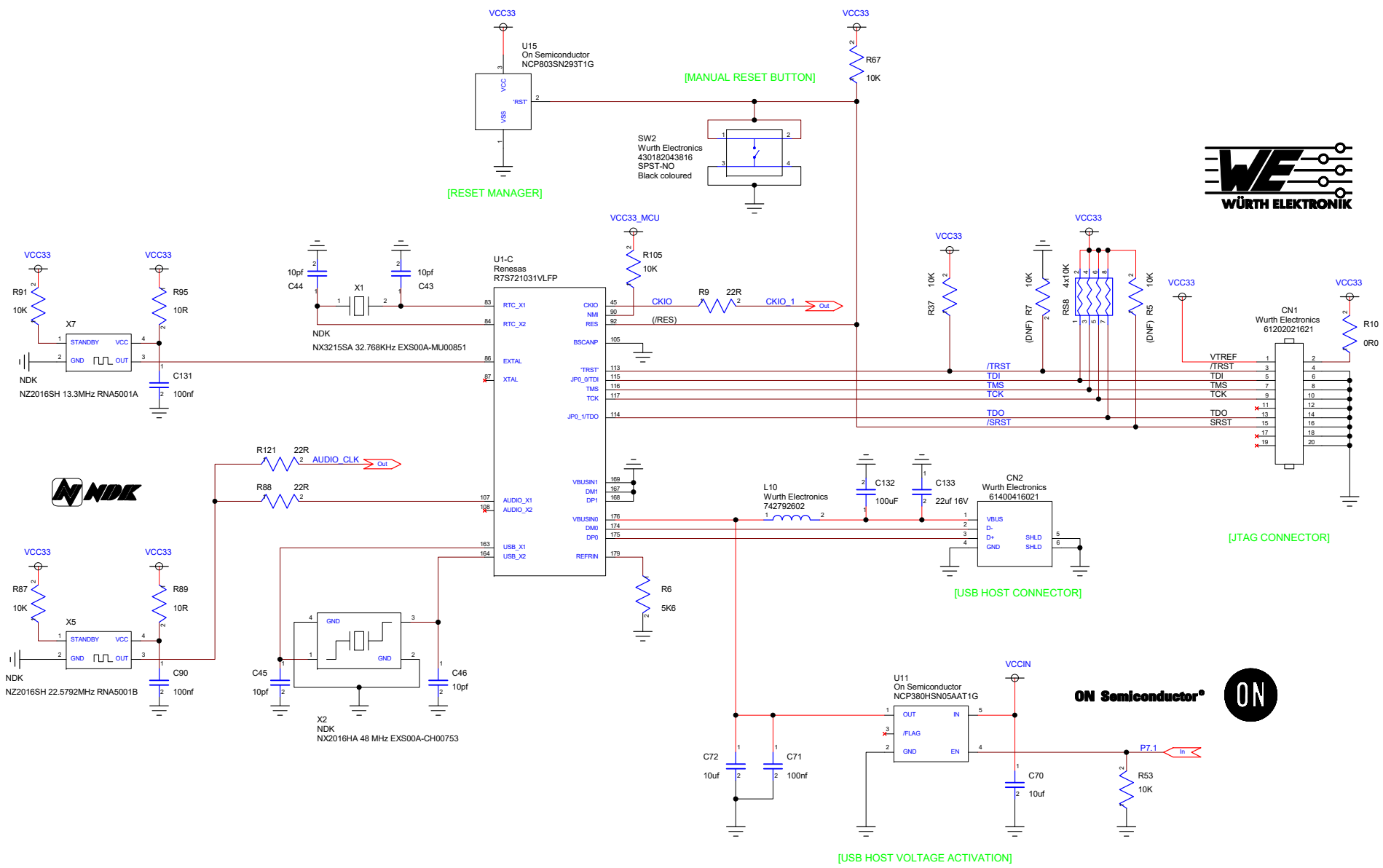
MD_CLKS	82	P3.3M0_CLKSRD3/SPDF_IN
MD_CLK	81	P3.2M0_CLKR0/IRQ7
MD_BOOT1	80	P3.1M0_BOOT1/RXD2SSRD3/ADTRG
MD_BOOT0	79	P3.0M0_BOOT0/RXD0
VIO_D7	101	P1.15AN7/IRQ7/ET_RXD3/VIO_D7
VIO_D6	102	P1.14AN6/IRQ6/ET_RXD2/VIO_D6
VIO_D5	99	P1.13AN5/IRQ5/ET_RXD1/VIO_D5
VIO_D4	98	P1.12AN4/IRQ4/ET_RXD0/VIO_D4
TFT_IRQ	97	P1.11AN3/IRQ3/RXD3/DV0_DATA7
AN2_POT10K	95	P1.10AN2/RXD2/DV0_DATA6
PMOD_IRQ0	94	P1.9AN1/RXD1/IRQ0/VIO_D4S
AUDIO_IRQ0 (P1.8/IRQ0)	94	P1.8AN0/RXD0/DV0_DATA4
VIO_D3	156	P1.7IRIC3SDA/RQ3/RXD2/VIO_D3
VIO_D2	155	P1.6IRIC2SDA/RQ2/SSIR0/DV0_D2
VIO_D1	154	P1.5IRIC1SDA/RQ1/VIO_D1
SDA1	153	P1.4IRIC0SDA/RQ0/RXD0/VIO_D0
SCL1	152	P1.3IRIC1SCL/RQ6/ET_RXD3/DV0_DATA3
SDA0	150	P1.2IRIC1SCL/RQ6/ET_RXD2/DV0_DATA2
SCL0	149	P1.1IRIC0SCL/RQ4/ET_RXD1/DV0_DATA1
		P1.0IRIC0SCL/RQ4/ET_RXD0/DV0_DATA0
CAM TFT_RST (P2.9)	161	P2.9A0/SSW3/SCSK0/IRQ1
CAM PWRDN (P2.8)	160	P2.8R0/RSSITd3/TIOCA
ET_RESETB (P2.7)	159	P2.7C30/SSSCK3/TIOCA/IRQ2
RDWR (P2.6)	158	P2.6R0/RVRS/SPRd3/TIOCA
DOMLU (P2.5)	112	P2.5V5W1Y/DV0/DQMLU/TIOCA
DOMLL (P2.4)	110	P2.4V5W0/DQMLU/TIOCA
CKE (P2.3)	76	P2.3CBE/CAN1/TXIOCD
/CAS (P2.2)	75	P2.2CAB/CAN1/RX/TIOCCIRG5
/RAS (P2.1)	68	P2.1YR1/RULR03/S/SPDF_OUT/IRQ6
/CS3 (P2.0)	68	P2.0CS3/RULR03/S/SPDF_IN/IRQ7
PMOD_RST	157	P3.15A16/VIO_FLD/DV0_DATA15/TXD1
P3.14	148	P3.14A15/VIO_CLK/SPDF_IN/DV0_DATA14/SK1A/AUDIO_XOUT2
P3.13	146	P3.13A14/SPBIO31_0/TIOCC3/DV0_DATA13
P3.12	144	P3.12A13/SPBIO21_0/TIOCC3/DV0_DATA12
P3.11	142	P3.11A12/SPBIO11_0/TIOCC3/DV0_DATA11
P3.10	141	P3.10A11/SPBIO01_0/TIOCC3/DV0_DATA10/RXD3
A10	139	P3.9A10/SPDF_OUT/DV0_DATA9/TXD3
A9	138	P3.8A9/AUDIO_CLK/DV0_DATA8/SCK3
A8	133	P3.7A8/SD_CD_0/LCDD0_DATA7/ET_CRS
A7	132	P3.6A7/SD_WP_0/LCDD0_DATA6/ET_COL
A6	131	P3.5A6/SD_D1_0/LCDD0_DATA5/ET_RXDV
A5	128	P3.4A5/SD_D0_0/LCDD0_DATA4/ET_RXER
A4	124	P3.3A4/SD_CLK_0/LCDD0_DATA3/ET_RXCLK
A3	122	P3.2A3/SD_CMD_0/LCDD0_DATA2/ET_TXEN
A2	120	P3.1A2/SD_D3_0/LCDD0_DATA1/ET_TXER
A1	119	P3.0A1/SD_D2_0/LCDD0_DATA0/ET_TXCLK
SPBIO10_0	204	P4.7A24/SPBIO10_0/TRACEDATA1
SPBIO00_0	202	P4.6A23/SPBIO00_0/TRACEDATA0
SPBSSL_0	197	P4.5A22/SPBSSL_0/TRACECTL
SPBCLK_0	196	P4.4A21/SPBCLK_0/TRACECLK
SPBIO30_0	191	P4.3A20/SPBIO30_0/TRACEDATA3
SPBIO20_0	190	P4.2A19/SPBIO20_0/TRACEDATA2
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VIO_VD	188	P4.0A17/VIO_VD/ET_MDIO/CTS1
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D14	15	P5.14D14/SSDATA2/RXD4/TIOCA2
D13	14	P5.13D13/SSWS2/AUDIO_XOUT/AUDIO_XOUT3
D12	13	P5.12D12/SSSCK2/SCK4/AUDIO_XOUT2
D11	12	P5.11D11/ETXD/TIOCCIRG6
D10	10	P5.10D10/ETRX/TIOCCIRG5
D9	8	P5.9D9/CAN0/TXIOCC4B/IRQ4
D8	6	P5.8D8/CAN0/RX/TIOCC4A/IRQ3
D7	5	P5.7D7/MISO2/SSIRd1/DV0_DATA23/TXD2
D6	4	P5.6D6/MISO2/SSSITXD1/DV0_DATA22/SCK2
D5	3	P5.5D5/SSL2/SSW1S1/DV0_DATA21
D4	2	P5.4D4/RSPCK2/SSSCK1/DV0_DATA20
D3	1	P5.3D3/MMC_D7/ET_TXD3/DV0_DATA19/LCDD0_TCON3
D2	208	P5.2D2/MMC_D6/ET_TXD2/DV0_DATA18/LCDD0_TCON2
D1	207	P5.1D1/MMC_D5/ET_TXD1/DV0_DATA17/LCDD0_TCON1
D0	205	P5.0D0/MMC_D4/ET_TXD0/DV0_DATA16/LCDD0_TCON0

D31/LCDD0_DATA23/MISO1/P8.15	49	MISO1
D30/LCDD0_DATA22/MOSI/SSDATA2/P8.14	48	MOSI1
D29/LCDD0_DATA21/SSL10/SSW2/P8.13	46	SSL10
D28/LCDD0_DATA20/RSPCK1/SSSCK2/P8.12	43	RSCK1
D27/LCDD0_DATA19/SSIRd0/SSDATA2/P8.11	41	SSIRx_D0
D26/LCDD0_DATA18/SSIRd0/RQ3/P8.10	40	SSITx_D0
D25/LCDD0_DATA17/SSW0/RQ2/P8.9	38	SSIW50
D24/LCDD0_DATA16/SSSCK0/RQ1/P8.8	33	SSISCK0
D23/LCDD0_DATA15/SSSRd3/RQ0/P8.7	32	LCDD0_DATA15
D22/LCDD0_DATA14/SSSRd3/MB_DAT/P8.6	31	LCDD0_DATA14
D21/LCDD0_DATA13/SSW5/MB_SIG/P8.5	26	LCDD0_DATA13
D20/LCDD0_DATA12/SSSCK3/MB_CLK/P8.4	24	LCDD0_DATA12
D19/LCDD0_DATA11/MISO0/CLK/P8.3	22	LCDD0_DATA11
D18/LCDD0_DATA10/MOSI0/CLK/P8.2	20	LCDD0_DATA10
D17/LCDD0_DATA9/SSL00/CLK/P8.1	19	LCDD0_DATA9
D16/LCDD0_DATA8/RSPCK0/CLK/VIO_VD/P8.0	17	LCDD0_DATA8
		P7.15
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		P7.13
		P7.12
		P7.11
		P7.10
		P7.9
		P7.8
		P7.7
		P7.6
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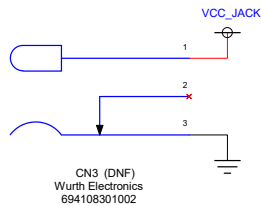
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		P5.0

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	PAGE	MCU - I/O			APPROVED BY	TOLENTINO M.	DATE	
<p>Designed by M13design www.m13design.fr</p>	REFERENCE	VERSION	REV	REMARKS		DATE	SIZE	SHEET
	REN0001 1402	V2.3		DNF : Dot Not Fit		2017.09.25	A4	02 OF 13

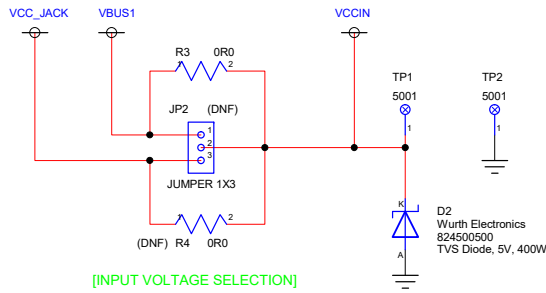




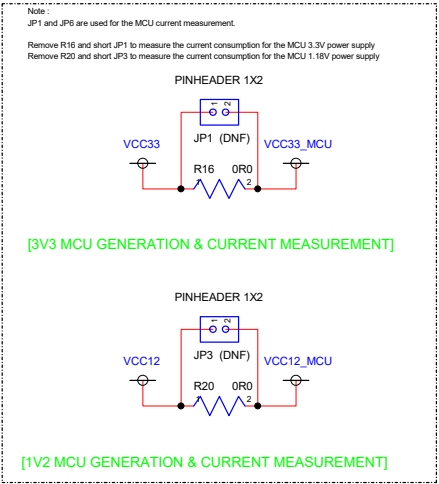
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	PAGE	MCU - OTHER CONNECTIONS				APPROVED BY	TOLENTINO M.	DATE		
 Designed by M3design www.m13design.fr	REFERENCE	VERSION	REV	REMARKS				DATE	SIZE	SHEET
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[JACK POWER SUPPLY]
[STRICTLY 5VDC]
[CENTER POSITIVE]

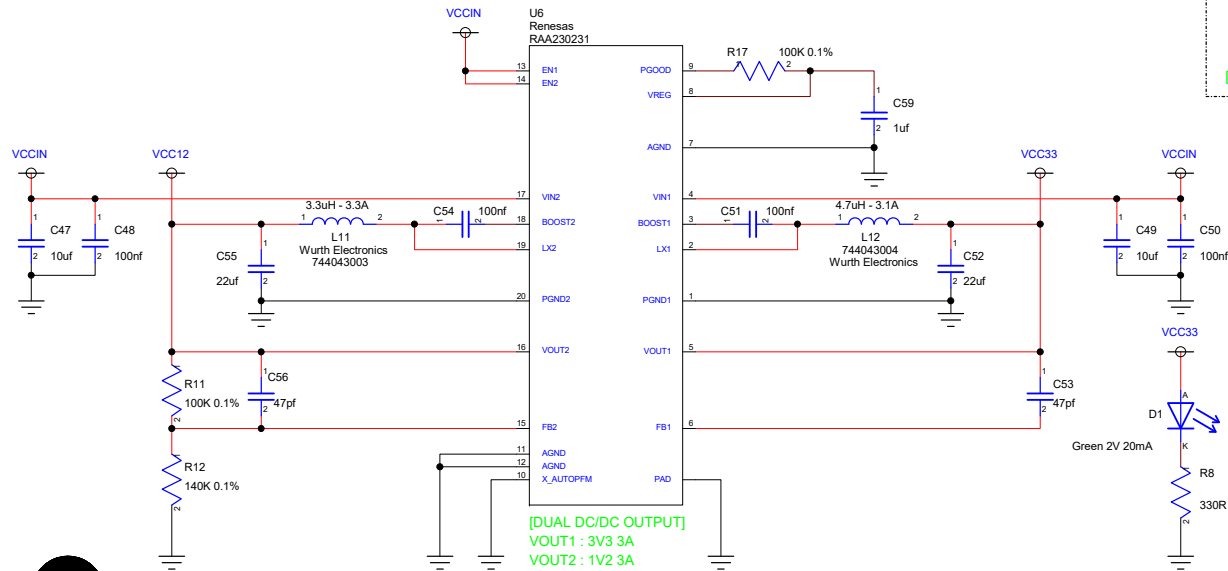


[INPUT VOLTAGE SELECTION]



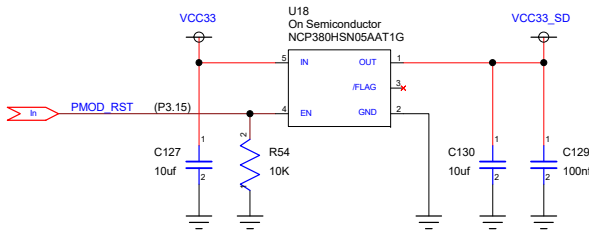
[3V3 MCU GENERATION & CURRENT MEASUREMENT]

[1V2 MCU GENERATION & CURRENT MEASUREMENT]

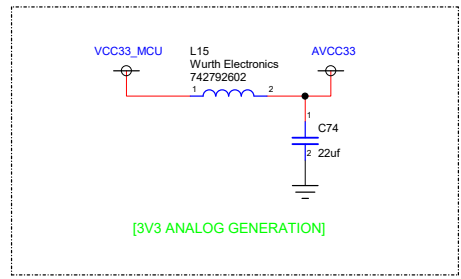


[DUAL DC/DC OUTPUT]
VOUT1 : 3V3 3A
VOUT2 : 1V2 3A

[POWER ON LED]

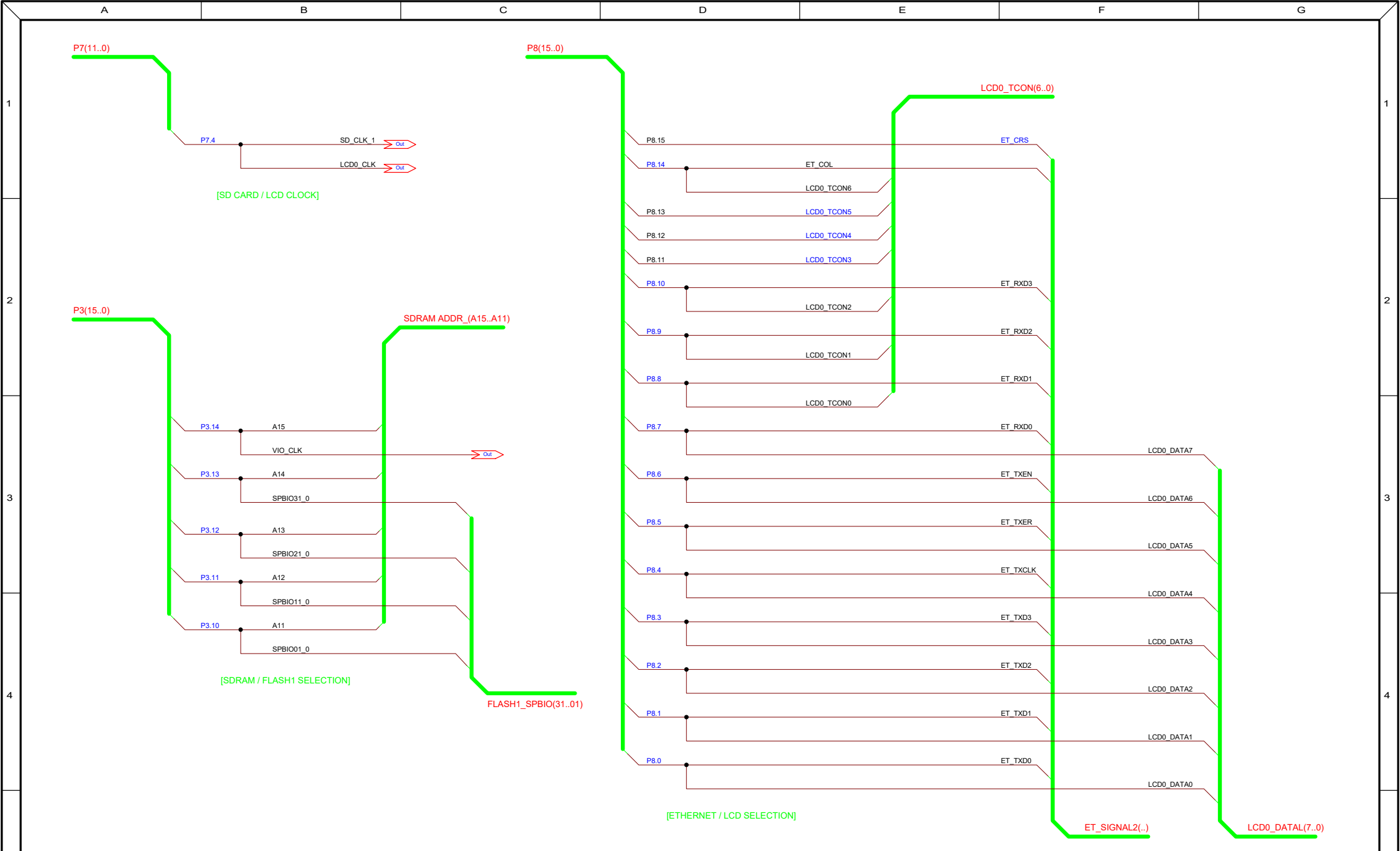


[SD-CARD POWER SUPPLY]



[3V3 ANALOG GENERATION]

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	PAGE	POWER SUPPLY				APPROVED BY	TOLENTINO M.	DATE	
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	REN0001 1402	V2.3		DNF : Dot Not Fit	DATE	2017.09.25	SIZE	A4	SHEET

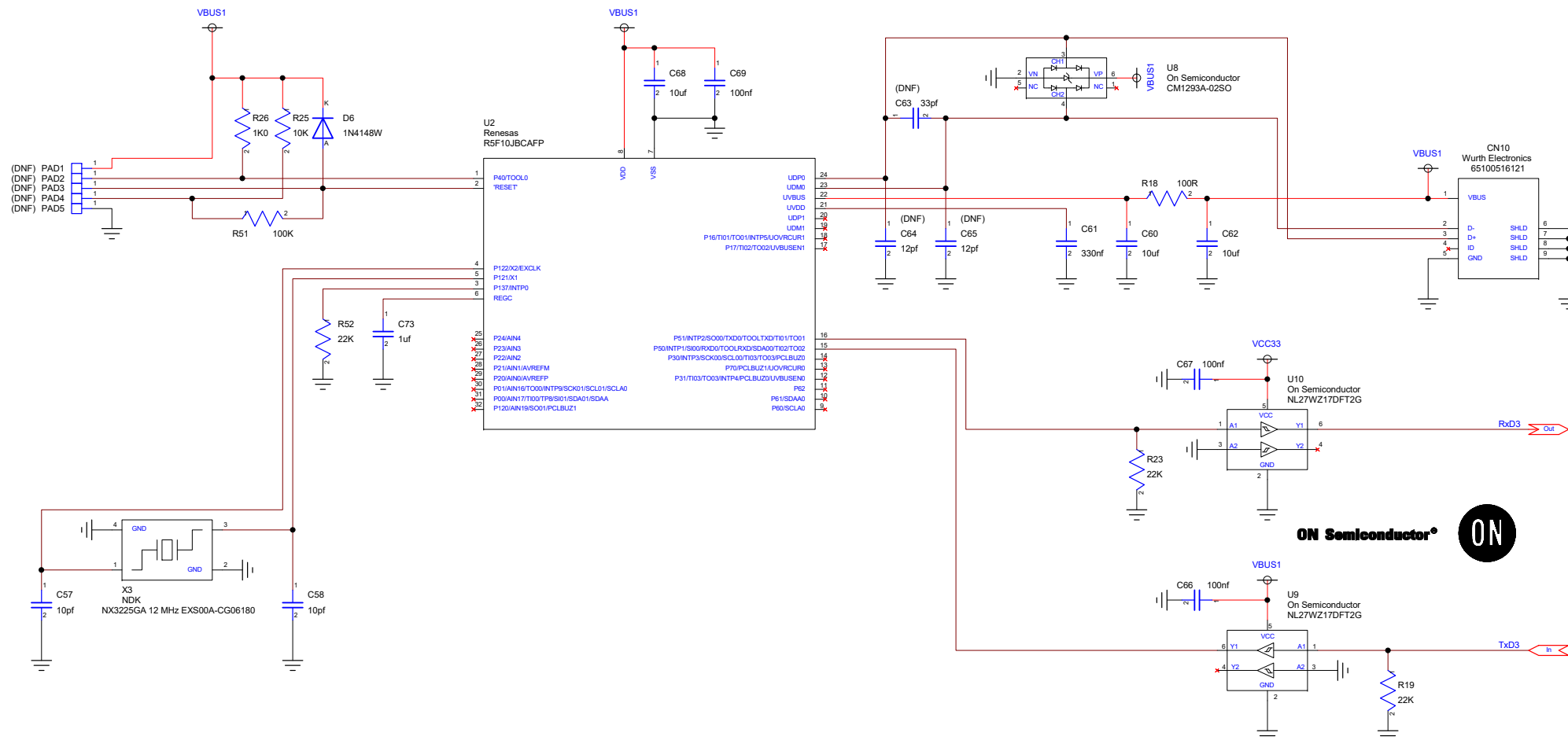


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PRODUCT	STREAM-IT - RZ/A1L BOARD LAYOUT			
PAGE	I/O FUNCTION SELECTION			
REFERENCE	VERSION	REV	REMARKS	
REN0001 1402	V2.3		DNF : Dot Not Fit	

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APPROVED BY	TOLENTINO M.	DATE	
		DATE	2017.09.25
		SIZE	A4
		SHEET	06 OF 13



U2
Renesas
R5F10JBCAFP

P40/TOCL0
RESET

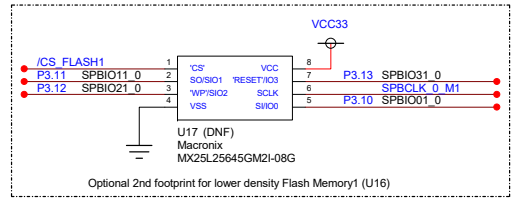
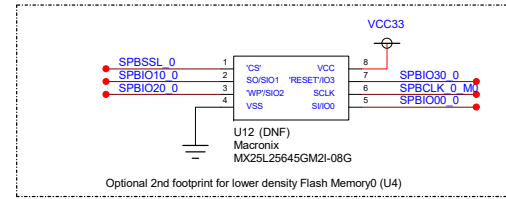
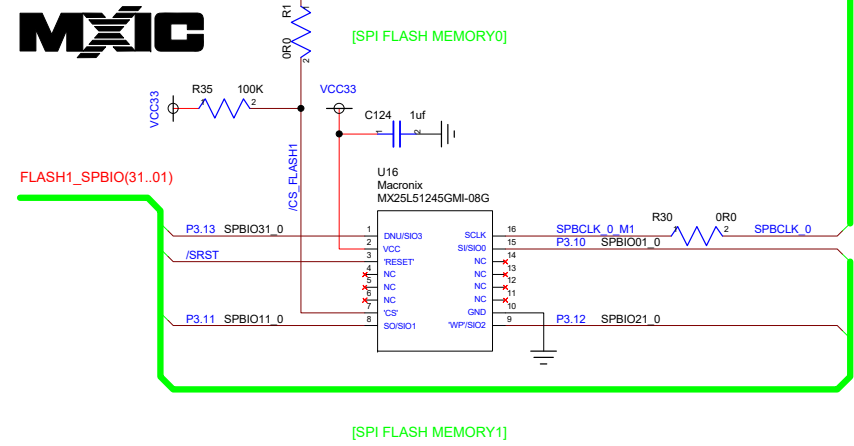
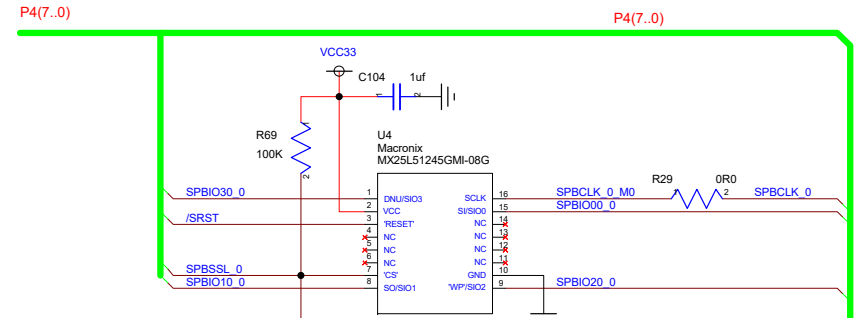
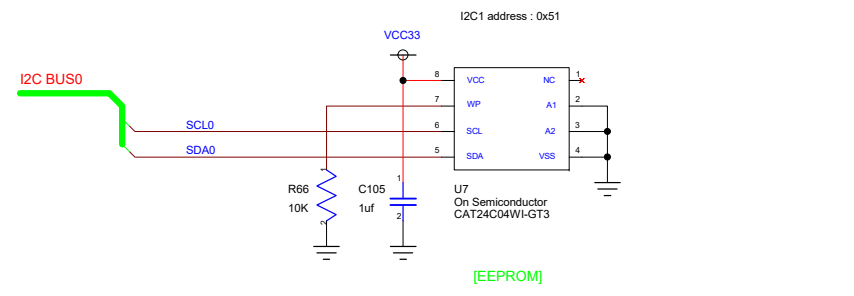
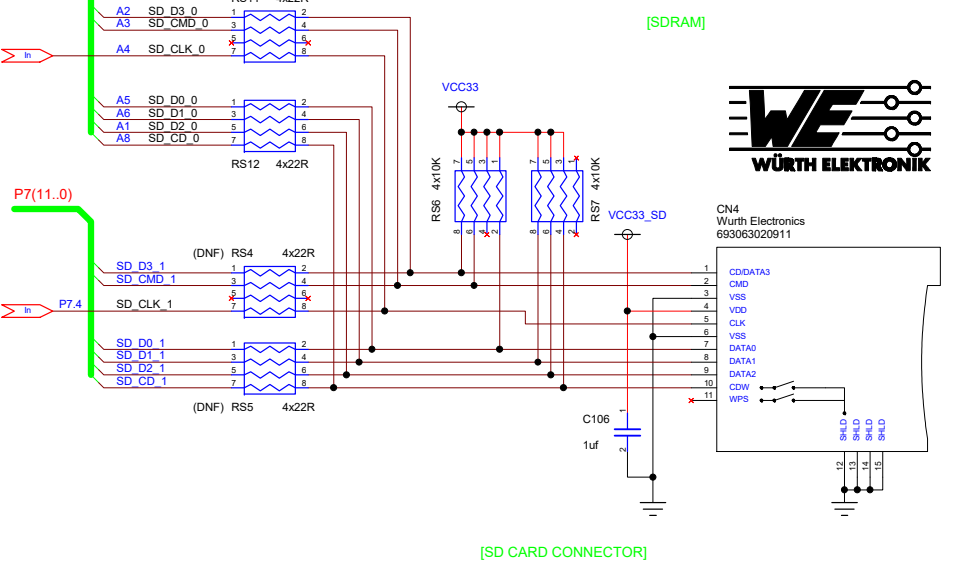
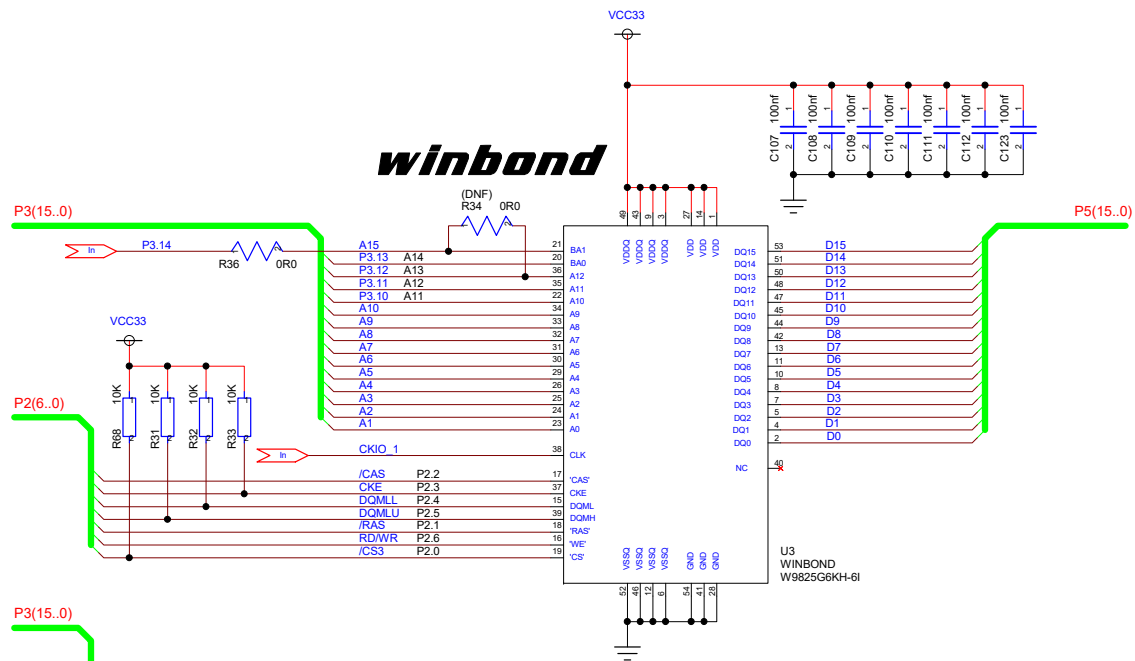
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UVBUS
LVDD
UDP1
UDM1
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P17/TIO2/TO02/UVBUSEN1

P122/X2/EXCLK
P121/IX1
P137/INTP0
REGC

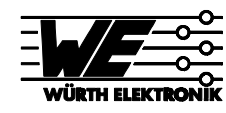
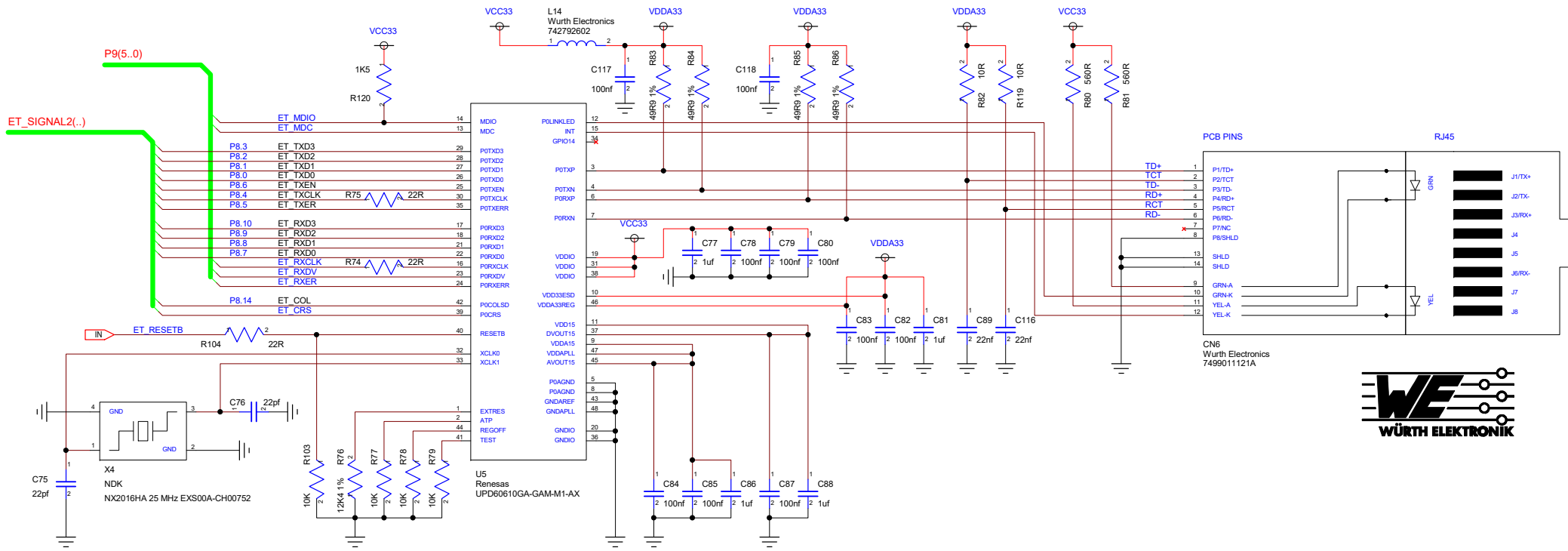
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P21/AIN1/AVREFM
P20/AIN0/AVREFP
P19/AIN7/TO00/INTP8/SCK01/SCL01/SCLA0
P00/AIN17/TIO0/TP8/SIO1/SDA01/SDAA
P120/AIN19/SO01/PCLBUZ1



P51/INTP2/SO00/TXD0/TOCLTXD/TIO1/TO01
P50/INTP1/SIO0/RXD0/TOCLRXD/SDA00/TIO2/TO02
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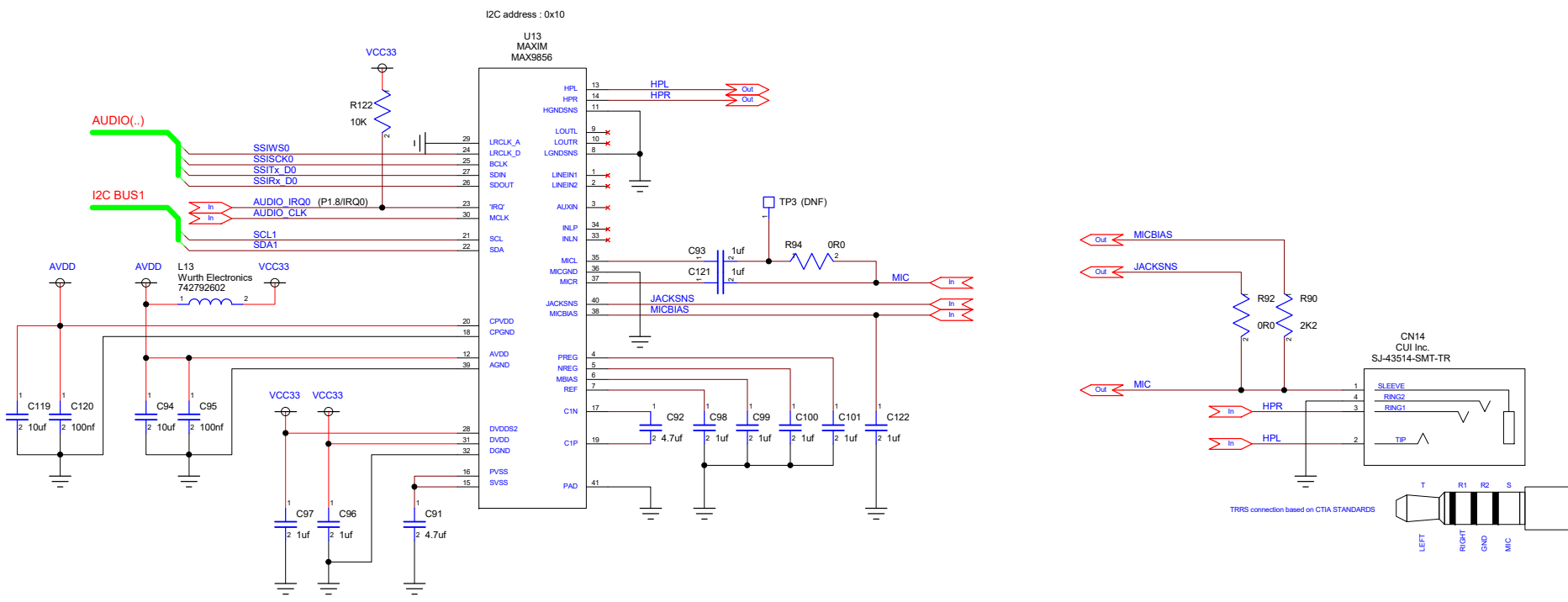
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<p>Designed by M3design www.m13design.fr</p>	REFERENCE	VERSION	REV	REMARKS			DATE	SIZE	SHEET
	REN0001 1402	V2.3		DNF : Dot Not Fit			2017.09.25	A4	07 OF 13



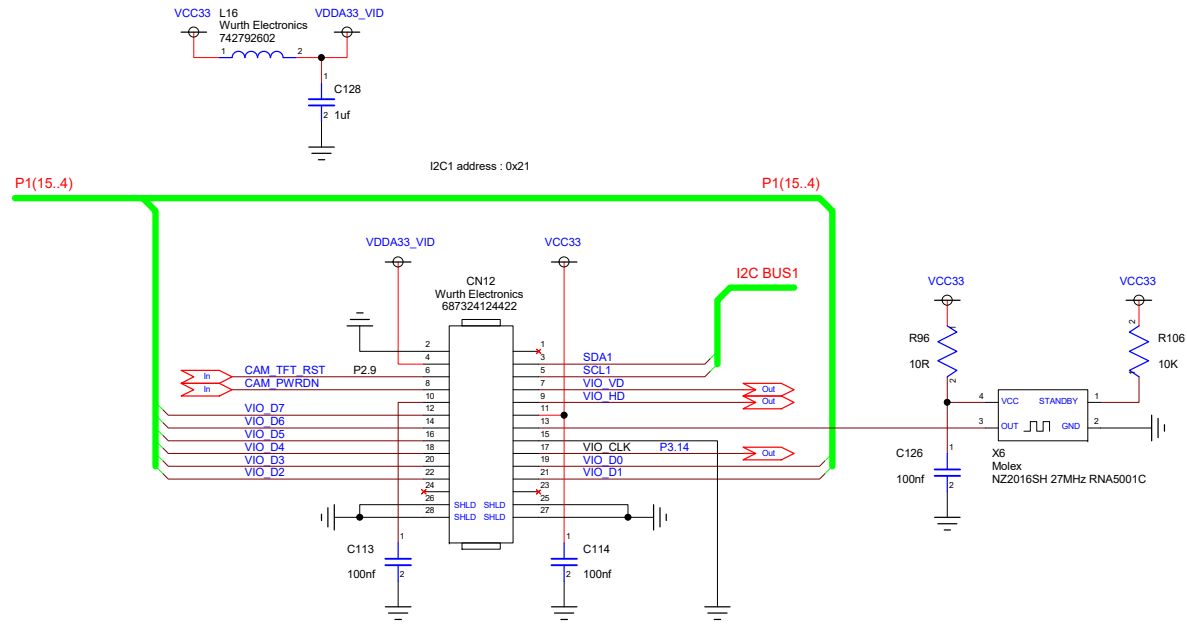
<p>Owned by RENASAS www.renesas.eu</p>	PRODUCT	STREAM-IT - RZ/A1L BOARD LAYOUT				DRAWN BY	PATRICK S.	DATE	2016.08.10
	PAGE	MEMORY - SD CARD				APPROVED BY	TOLENTINO M.	DATE	
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	REN0001 1402	V2.3		DNF : Dot Not Fit		2017.09.25	A4	08 OF 13	



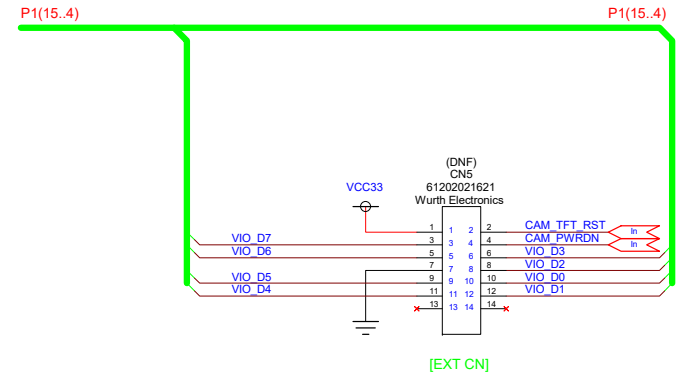
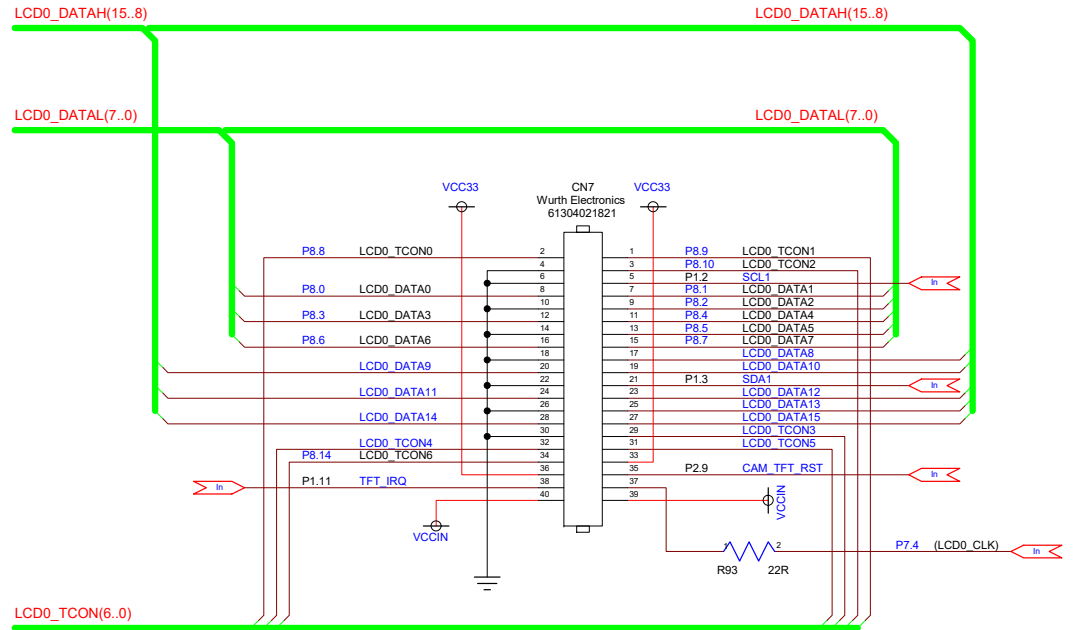
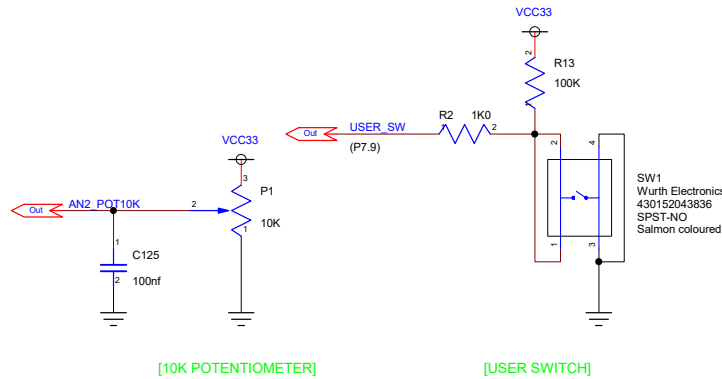
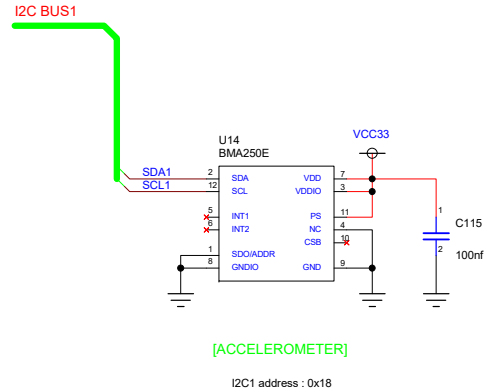
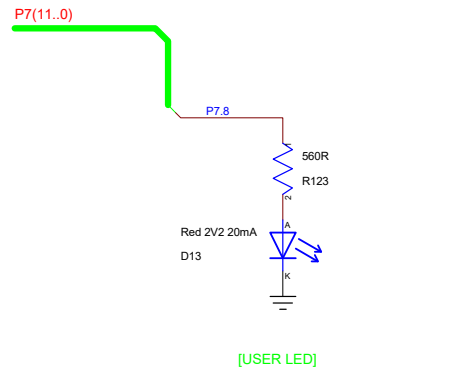
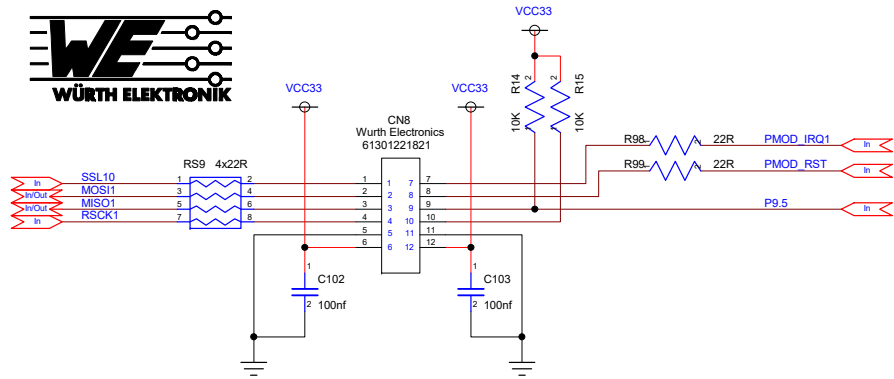
 Owned by RENESAS www.renesas.eu	PRODUCT	STREAM-IT - RZ/A1L BOARD LAYOUT				DRAWN BY	PATRICK S.	DATE	2016.08.10	
	PAGE	ETHERNET				APPROVED BY	TOLENTINO M.	DATE		
 Designed by M3design www.m13design.fr	REFERENCE	VERSION	REV	REMARKS				DATE	SIZE	SHEET
	REN0001 1402	V2.3		DNF : Dot Not Fit				2017.09.25	A4	09 OF 13





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	PAGE	AUDIO				APPROVED BY	TOLENTINO M.	DATE	
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VERSION	REVISION	DATE	DESCRIPTION
0.1		2014/08/27	FIRST DRAFT
1.0		2015/08/25	CONNECT RZ (U1) PIN103 TO GND, CONNECT C16 & C17 TO GND
2.0		2016/02/10	ADDED CURRENT CONSUMPTION ON 3V3 AND 1V2, REMOVED RS1/RSS3, REPLACED AUDIO/MIC CONNECTORS WITH A SINGLE AUDIO/MIC CONNECTOR, U4 IS MOUNTED BY DEFAULT, DNF DISPLAYED REMOVED PULLUPS ON FLASH IO, DCDC AND P1.11 FOR SD CARD, USER SWITCH MOVED TO P7.9, ADDED 13.33MHZ ON EXTAL, JUMPER SELECTION ON BOOT
2.1		2016/08/26	MOVED TFT_IRQ TO P1.11, SD POWER ENABLE PIN SHARED WITH PMOD_RST (P3.15), UPDATED U4/U16 MPN
2.2		2016/12/06	VBUSIN1 / DM1 & DP1 CONNECTED TO USBDPVSS (GND), C63 / C64 / C65 MARQUED AS DNF, ADDED 22R DAMPING RESISTOR ON BOTH QSPI CLK, CHANGED C61 TO 330NF C73 VALUE CHANGE TO 1UF, 100UF FILTER CAPACITOR ADDED ON USB HOST VBUS + AN EXTRA 0805 FOOTPRINT
2.2	A	2017/02/24	UPDATED U7 FROM CAT24C02W1-GT3 TO CAT24C04W1-GT3, REPLACED R28/R30 WITH 0R RESISTORS
2.3		2017/09/25	GND ON U10.3 & U8.3 / 10K PULL-UP ON OKE, DQMLL, DQMLU, REMOVED DNF STATUS ON C133, C133 VALUE CHANGED TO 22UF-10V / DISCONNECTED VCC33 FROM U7.1 / UPDATED U7.1 PIN DESCRIPTION TO "NC" ADDED R34 OR BETWEEN U3.21 & U3.36 AS DNF / ADDED 100K PULLUP R35 ON U16.7 (CS) / ADDED R36 IN LINE ON P3.14 SIGNAL / R5 AS DNF / ADDED R37 10K PULLUP ON TRST / RT AS DNF

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